Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A hybrid built-in self test (BIST) architecture for embedded memory arrays that segments BIST functionality into remote lower-speed executable instructions and local higher-speed executable instructions, the architecture comprising:

a standalone BIST logic controller operating at a lower frequency and being adapted to communicate with a plurality of embedded memory arrays using a BIST instruction set; and

a block of higher-speed test logic incorporated into each embedded memory array under test and being adapted to locally process BIST instructions received from said standalone BIST logic controller at a higher frequency than said lower frequency.

[c2] 2.The hybrid BIST architecture in claim 1, wherein said higher-speed test logic includes a multiplier for increasing the frequency of said BIST instructions from said lower frequency to said higher frequency.

[c3] 3.The hybrid BIST architecture in claim 1, wherein said standalone BIST logic controller enables a plurality of

higher-speed test logic structures in a plurality of embedded memory arrays.

[c4] 4.The hybrid BIST architecture in claim 1, wherein said standalone logic controller enables testing of different types of embedded memories.

[c5] 5.The hybrid BIST architecture in claim 1, further comprising a lower-speed control bus operating at said lower frequency and connecting said standalone BIST logic controller to said higher-speed test logic.

[c6] 6.The hybrid BIST architecture in claim 1, wherein said standalone BIST logic controller comprises at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets.

[c7] 7.The hybrid BIST architecture in claim 1, wherein said standalone BIST logic controller comprises logic adapted to provide branch prediction, program counter management, utility counters, and general BIST operation controls and diagnostic outputs.

[c8] 8.A built-in self test (BIST) architecture for use with memory arrays embedded in functional circuitry within an integrated circuit, said BIST architecture comprising: a plurality of embedded blocks of test logic incorporated

into embedded memory arrays;
a remote BIST logic controller, separate from said embedded blocks of test logic; and
a bus connecting said remote BIST logic controller to said embedded blocks of test logic,
wherein said remote BIST logic controller performs functions that are common to all of said embedded blocks of test logic, and
wherein said remote BIST logic controller and said bus operate at a lower frequency than said embedded blocks of test logic.

[c9] 9.The BIST architecture in claim 8, wherein said embedded blocks of test logic each include a multiplier for increasing the frequency of BIST instructions received from said BIST logic controller to a higher frequency of a corresponding embedded memory array.

[c10] 10.The BIST architecture in claim 8, wherein each of said embedded blocks of test logic includes unique logic blocks that are unique to a corresponding embedded memory array.

[c11] 11.The BIST architecture in claim 8, wherein each of said embedded blocks of test logic includes:
a clock multiplier;
redundancy allocation logic;

data address control generation logic; and
decoding logic adapted to decode macro instruction sets received from said remote BIST logic controller into multiple individual micro instructions.

[c12] 12.The BIST architecture in claim 8, wherein said remote BIST logic controller enables testing of different types of embedded memories.

[c13] 13.The BIST architecture in claim 8, wherein said standalone BIST logic controller comprises at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets.

[c14] 14.The BIST architecture in claim 8, wherein said remote BIST logic controller comprises logic adapted to provide branch prediction, program counter management, utility counters, and general BIST operation controls and diagnostic outputs.

[c15] 15.A built-in self test (BIST) architecture for use with memory arrays embedded in functional circuitry within an integrated circuit, said BIST architecture comprising:
a plurality of embedded blocks of test logic incorporated into embedded memory arrays;
a remote BIST logic controller, separate from said em-

bedded blocks of test logic; and

a bus connecting said remote BIST logic controller to said embedded blocks of test logic, wherein said remote BIST logic controller and said bus operate at a lower frequency than said embedded blocks of test logic, and wherein said remote BIST logic controller performs functions that are common to all of said embedded blocks of test logic including providing branch prediction, program counter management, utility counting, and general BIST operation control and diagnostic outputs.

[c16] 16.The BIST architecture in claim 15, wherein said embedded blocks of test logic each include a multiplier for increasing the frequency of BIST instructions received from said BIST logic controller to a higher frequency of a corresponding embedded memory array.

[c17] 17.The BIST architecture in claim 15, wherein each of said embedded blocks of test logic includes unique logic blocks that are unique to a corresponding embedded memory array.

[c18] 18.The BIST architecture in claim 15, wherein each of said embedded blocks of test logic includes:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic adapted to decode macro instruction sets received from said remote BIST logic controller into multiple individual micro-instructions.

[c19] 19.The BIST architecture in claim 15, wherein said remote BIST logic controller enables testing of different types of embedded memories.

[c20] 20.The BIST architecture in claim 15, wherein said standalone BIST logic controller comprises at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets.

[c21] 21.The BIST architecture in claim 15, wherein said remote BIST logic controller comprises logic adapted to provide branch prediction, program counter management, utility counters, and general BIST operation controls and diagnostic outputs.

[c22] 22.A method of testing memory arrays embedded in functional circuitry within an integrated circuit using a built-in self test (BIST) architecture, said method comprising:
performing BIST test functions that are common to embedded blocks of test logic incorporated into each embedded memory array using a remote BIST logic con-

troller, separate from said embedded blocks of test logic;

sending BIST instructions from said remote BIST logic controller to said embedded blocks of test logic; and

increasing the frequency of BIST instructions received from said BIST logic controller, using said embedded blocks of test logic, to a higher frequency of a corresponding embedded memory array.

[c23] 23.The method in claim 22, wherein said sending of BIST instructions from said remote BIST logic controller to said embedded blocks of test logic uses a bus connecting said remote BIST logic controller to said embedded blocks of test logic, wherein said bus operates at the same frequency as said remote BIST logic controller.

[c24] 24.The method in claim 22, further comprising performing unique testing via logic blocks that are unique to a corresponding embedded memory array at each of said embedded blocks of test logic.

[c25] 25.The method in claim 22, wherein each of said embedded blocks of test logic performs the following processes:

multiplying BIST instructions received from said remote BIST logic controller;

performing redundancy allocation;

performing data address control and generation; and decoding macro instruction sets received from said remote BIST logic controller into individual instructions.

[c26] 26.The method in claim 22, wherein said sending process performed by said remote BIST logic controller enables testing of different types of embedded memories.

[c27] 27.The method in claim 22, further comprising storing macro instruction sets in one of read only memories (ROMs), a scannable read only memory (SROM), and other type of memory in said remote BIST logic controller.

[c28] 28.The method in claim 22, further comprising providing, by said remote BIST logic controller:
branch prediction;
program counter management;
utility counting; and
general BIST operation control and diagnostic outputs.

[c29] 29.A method of testing memory arrays embedded in functional circuitry within an integrated circuit using a built-in self test (BIST) architecture, said method comprising:
performing BIST test functions that are common to embedded blocks of test logic incorporated into each em-

bedded memory array using a remote BIST logic controller that operates at a first frequency, wherein said remote BIST logic controller is separate from said embedded blocks of test logic;
sending BIST instructions from said remote BIST logic controller to said embedded blocks of test logic at said first frequency; and
increasing the frequency of BIST instructions received from said BIST logic controller, using said embedded blocks of test logic, to a second frequency higher than said first frequency.

[c30] 30.The method in claim 29, wherein said sending of BIST instructions from said remote BIST logic controller to said embedded blocks of test logic uses a bus connecting said remote BIST logic controller to said embedded blocks of test logic.

[c31] 31.The method in claim 29, further comprising performing unique testing via logic blocks that are unique to a corresponding embedded memory array at each of said embedded blocks of test logic.

[c32] 32.The method in claim 29, wherein each of said embedded blocks of test logic performs the following processes:
multiplying BIST instructions received from said remote

BIST logic controller;
performing redundancy allocation;
performing data address control and generation; and
decoding macro instruction sets received from said remote BIST logic controller into individual instructions.

[c33] 33.The method in claim 29, wherein said sending process performed by said remote BIST logic controller enables testing of different types of embedded memories.

[c34] 34.The method in claim 29, further comprising storing macro instruction sets in one of read only memories (ROMs), a scannable read only memory (SROM), and other type of memory in said remote BIST logic controller.

[c35] 35.The method in claim 29, further comprising providing, by said remote BIST logic controller:
branch prediction;
program counter management;
utility counting; and
general BIST operation control and diagnostic outputs.